WHAT IS CLAIMED IS:

1. A semiconductor device having at least three or more power terminals superimposed on each other, and at least one semiconductor chip is connected electrically in a way to be sandwiched between predetermined two power terminals among said power terminals, in a semiconductor device for large power.

2. The semiconductor device according to claim 1, wherein a power terminal on one end among said superposed power terminals and a power terminal on the other end among said superposed power terminals are led out in the same direction.

3. The semiconductor device according to claim 2, wherein a power terminal positioned at the middle among said superposed power terminals is led out in a direction opposite to or perpendicular to a power terminal on said one or other end.

4. The semiconductor device according to claim 1, wherein one face of said at least one semiconductor chip sandwiched between said two power terminals is connected to one power terminal of said two power terminals by soldering or pressure welding, and the other face is connected to the other power terminal of said two power terminals by soldering or pressure welding through a buffer plate.

5. The semiconductor device according to claim 1, wherein said at least one semiconductor chip operates,

so that the current flows in the opposite direction for the power terminal on one end among said superposed power terminals and for the power terminal on the other end.

6. The semiconductor device according to claim 1, wherein said at least one semiconductor chip sandwiched between said power terminals is made of a plurality of semiconductor chips, and an insulation layer is provided among said semiconductor chips.

7. The semiconductor device according to claim 6, wherein said plurality of semiconductor chips comprises at least one transistor, and at least diode, and a control electrode is connected to said transistor

8. The semiconductor device according to claim 7, wherein said control electrode and a control electrode pad of said transistor are connected by wire bonding, or connected directly by sandwiching a buffer plate.

9. The semiconductor device according to claim 7, wherein said control electrode is led out in a direction opposite to or perpendicular to a power terminal positioned on one end of said power terminal or on the other end of said power terminal.

10. The semiconductor device according to claim 4, wherein the power terminals positioned on one end of said power terminal and the power terminal on the other end have a screw fixing structure so as to connect semiconductor chips by pressure welding between any two

power terminals of said power terminals superimposed on each other.